FIG. 1

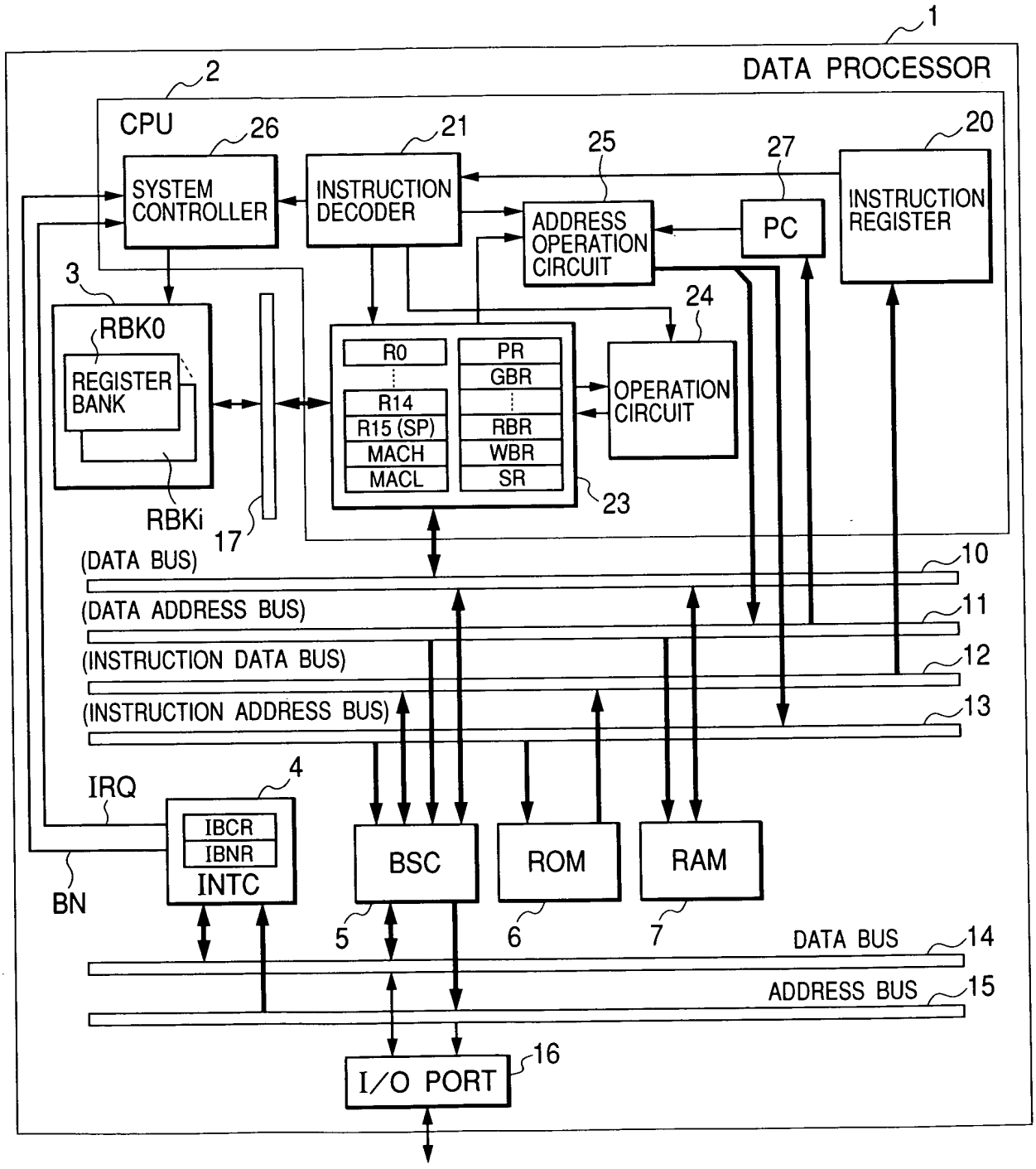
1
DATA PROCESSOR
2
CPU
26
SYSTEM CONTROLLER
21
INSTRUCTION DECODER
25
ADDRESS OPERATION CIRCUIT
27
PC
20
INSTRUCTION REGISTER
3
RBK0
REGISTER BANK
RBKi
17
24
R0
R14
R15 (SP)
MACH
MACL
PR
GBR
RBR
WBR
SR
23
OPERATION CIRCUIT
(DATA BUS)
10
(DATA ADDRESS BUS)
11
(INSTRUCTION DATA BUS)
12
(INSTRUCTION ADDRESS BUS)
13
IRQ
4
IBCR
IBNR
INTC
BN
BSC
ROM
RAM
5
6
7
DATA BUS
14
ADDRESS BUS
15
I/O PORT
16

FIG. 2

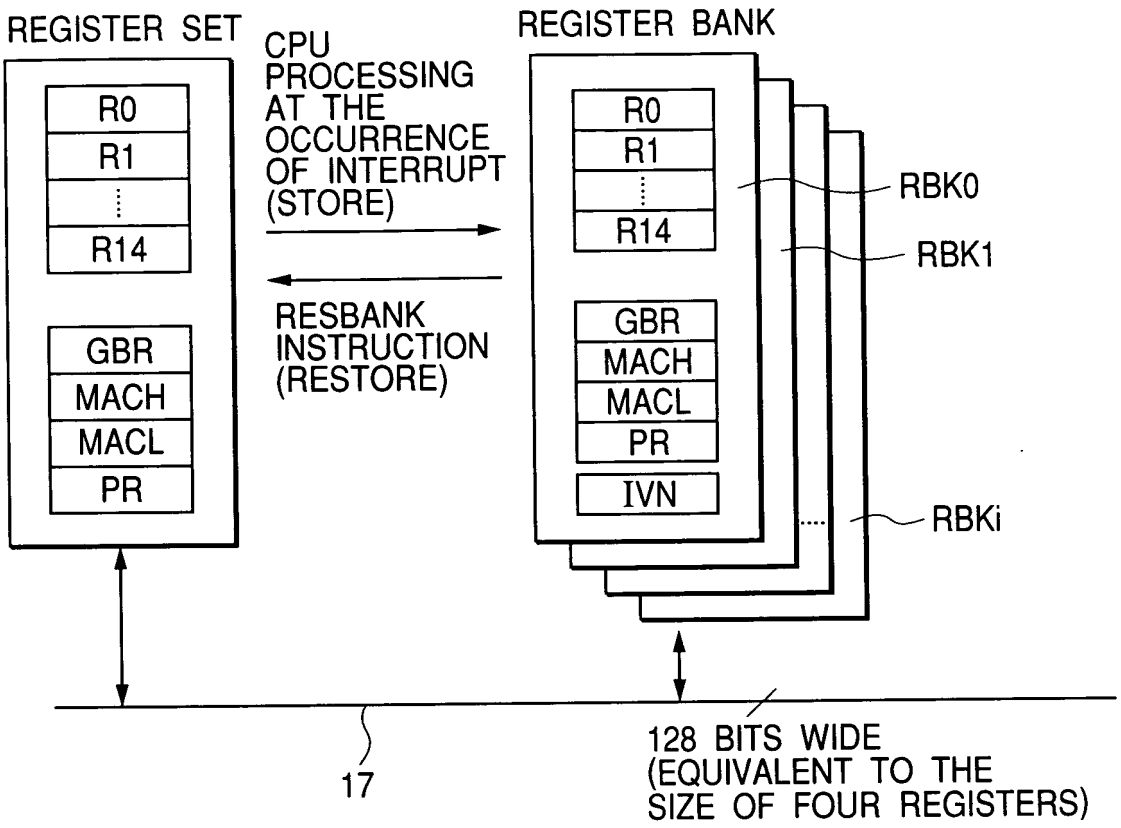
REGISTER SET
R0
R1
R14
GBR
MACH
MACL
PR
CPU PROCESSING AT THE OCCURRENCE OF INTERRUPT (STORE)
RESBANK INSTRUCTION (RESTORE)
REGISTER BANK
R0
R1
R14
GBR
MACH
MACL
PR
IVN
RBK0
RBK1
RBKi
17
128 BITS WIDE (EQUIVALENT TO THE SIZE OF FOUR REGISTERS)

FIG. 3

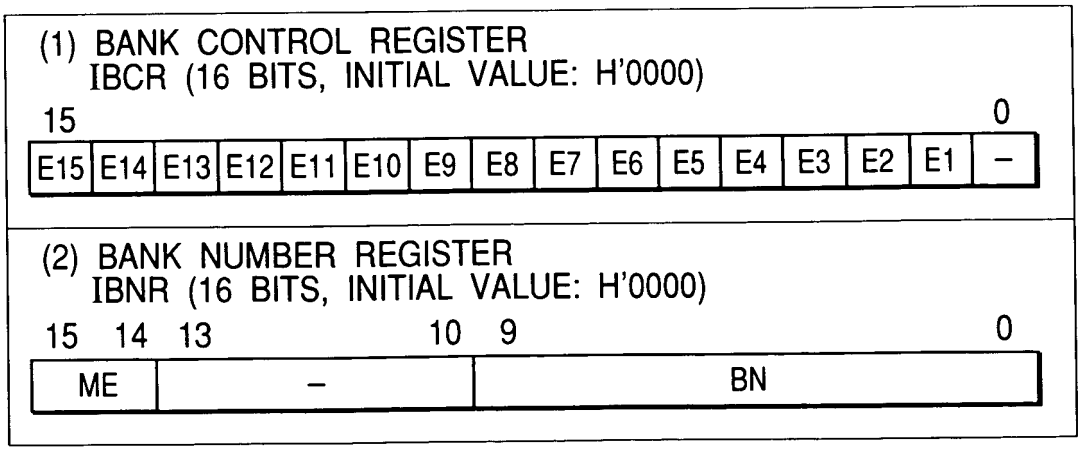
(1) BANK CONTROL REGISTER
IBCR (16 BITS, INITIAL VALUE: H'0000)
15
0
E15 E14 E13 E12 E11 E10 E9 E8 E7 E6 E5 E4 E3 E2 E1 –
(2) BANK NUMBER REGISTER
IBNR (16 BITS, INITIAL VALUE: H'0000)
15 14 13 10 9 0
ME
–
BN

FIG. 4

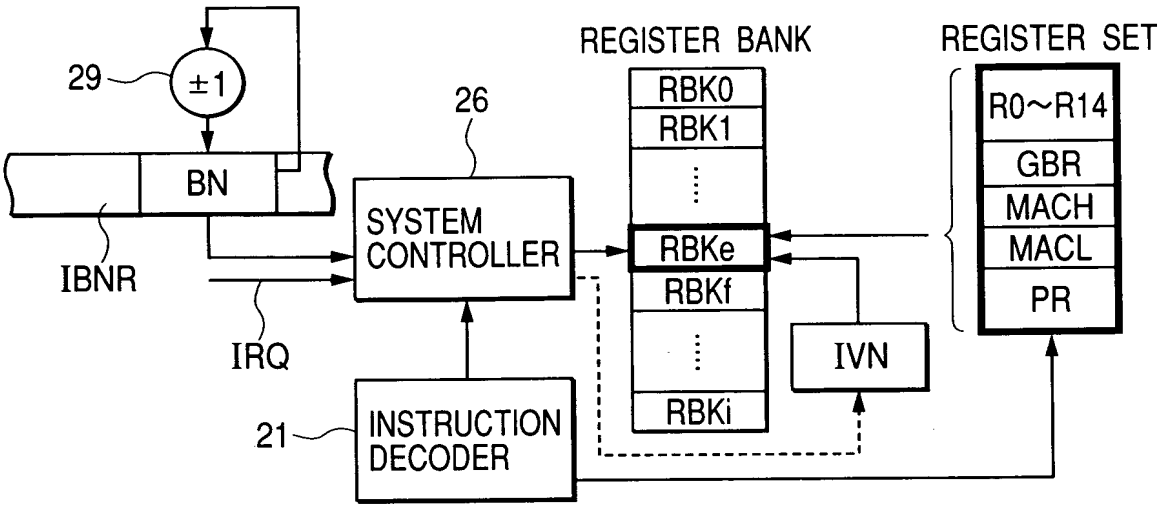
29
±1
BN
IBNR
IRQ
26
SYSTEM CONTROLLER
21
INSTRUCTION DECODER
REGISTER BANK
RBK0
RBK1
RBKe
RBKf
RBKi
IVN
REGISTER SET
R0~R14
GBR
MACH
MACL
PR

FIG. 5

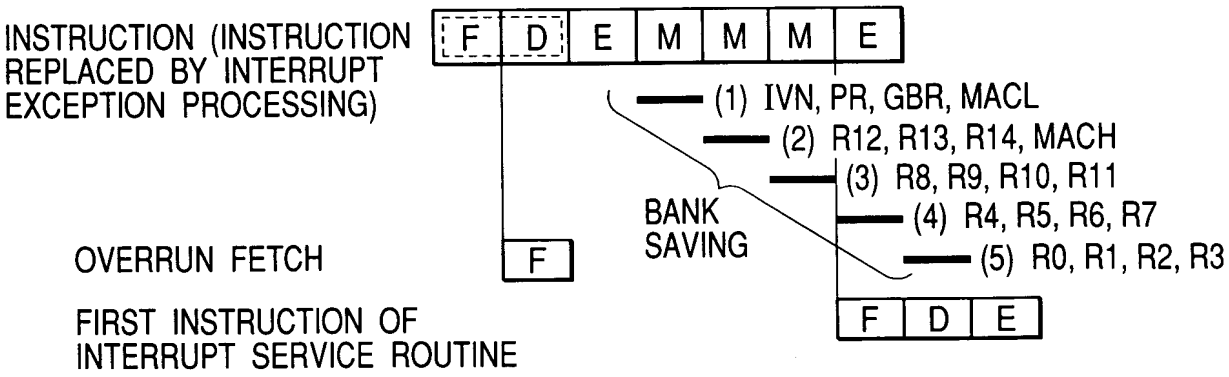
INSTRUCTION (INSTRUCTION REPLACED BY INTERRUPT EXCEPTION PROCESSING)
F
D
E
M
M
M
E
(1) IVN, PR, GBR, MACL
(2) R12, R13, R14, MACH
(3) R8, R9, R10, R11
(4) R4, R5, R6, R7
(5) R0, R1, R2, R3
BANK SAVING
OVERRUN FETCH
F
FIRST INSTRUCTION OF INTERRUPT SERVICE ROUTINE
F
D
E

FIG. 6

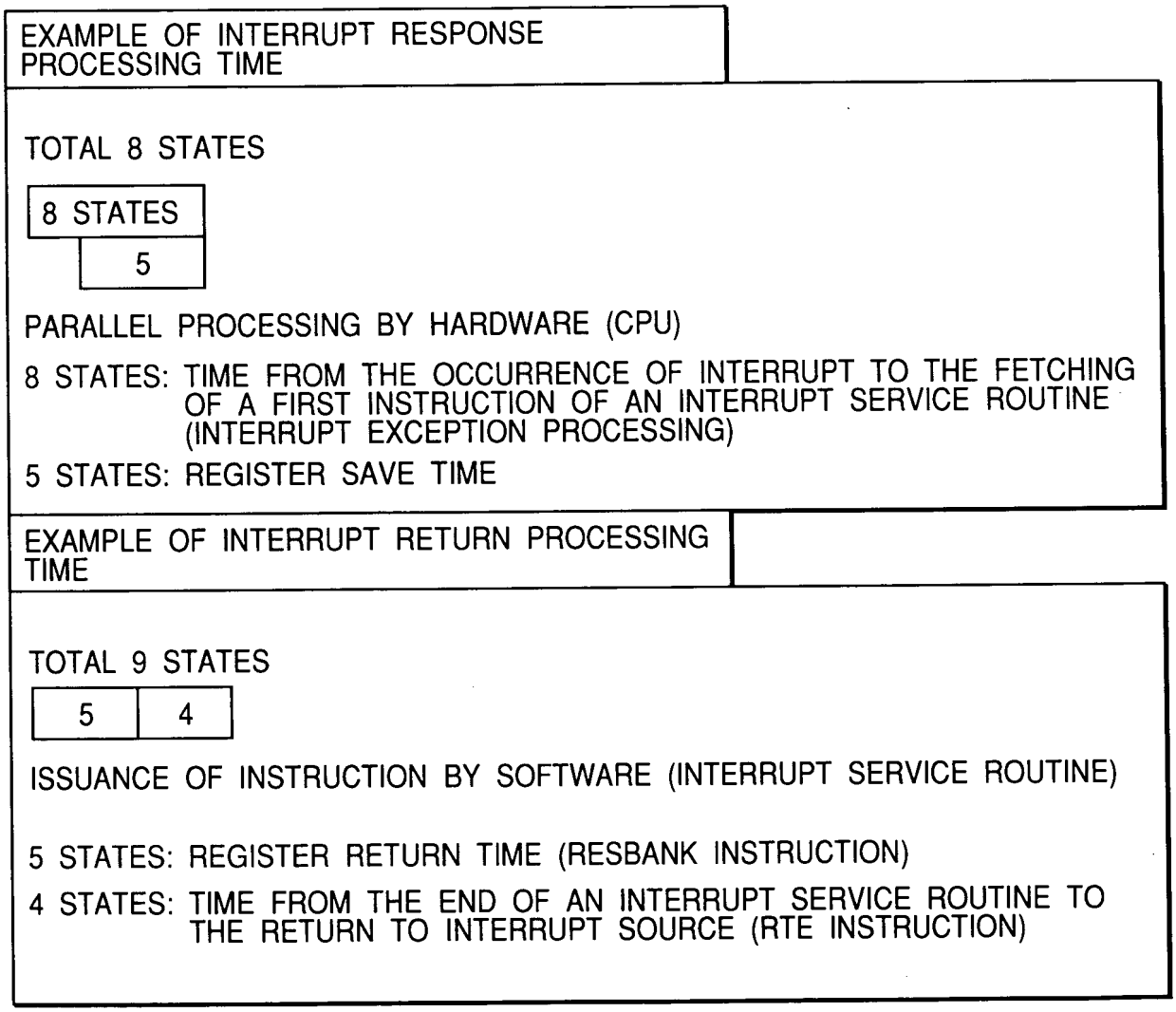
EXAMPLE OF INTERRUPT RESPONSE PROCESSING TIME
TOTAL 8 STATES
8 STATES
5
PARALLEL PROCESSING BY HARDWARE (CPU)
8 STATES: TIME FROM THE OCCURRENCE OF INTERRUPT TO THE FETCHING OF A FIRST INSTRUCTION OF AN INTERRUPT SERVICE ROUTINE (INTERRUPT EXCEPTION PROCESSING)
5 STATES: REGISTER SAVE TIME
EXAMPLE OF INTERRUPT RETURN PROCESSING TIME
TOTAL 9 STATES
5
4
ISSUANCE OF INSTRUCTION BY SOFTWARE (INTERRUPT SERVICE ROUTINE)
5 STATES: REGISTER RETURN TIME (RESBANK INSTRUCTION)
4 STATES: TIME FROM THE END OF AN INTERRUPT SERVICE ROUTINE TO THE RETURN TO INTERRUPT SOURCE (RTE INSTRUCTION)

FIG. 7

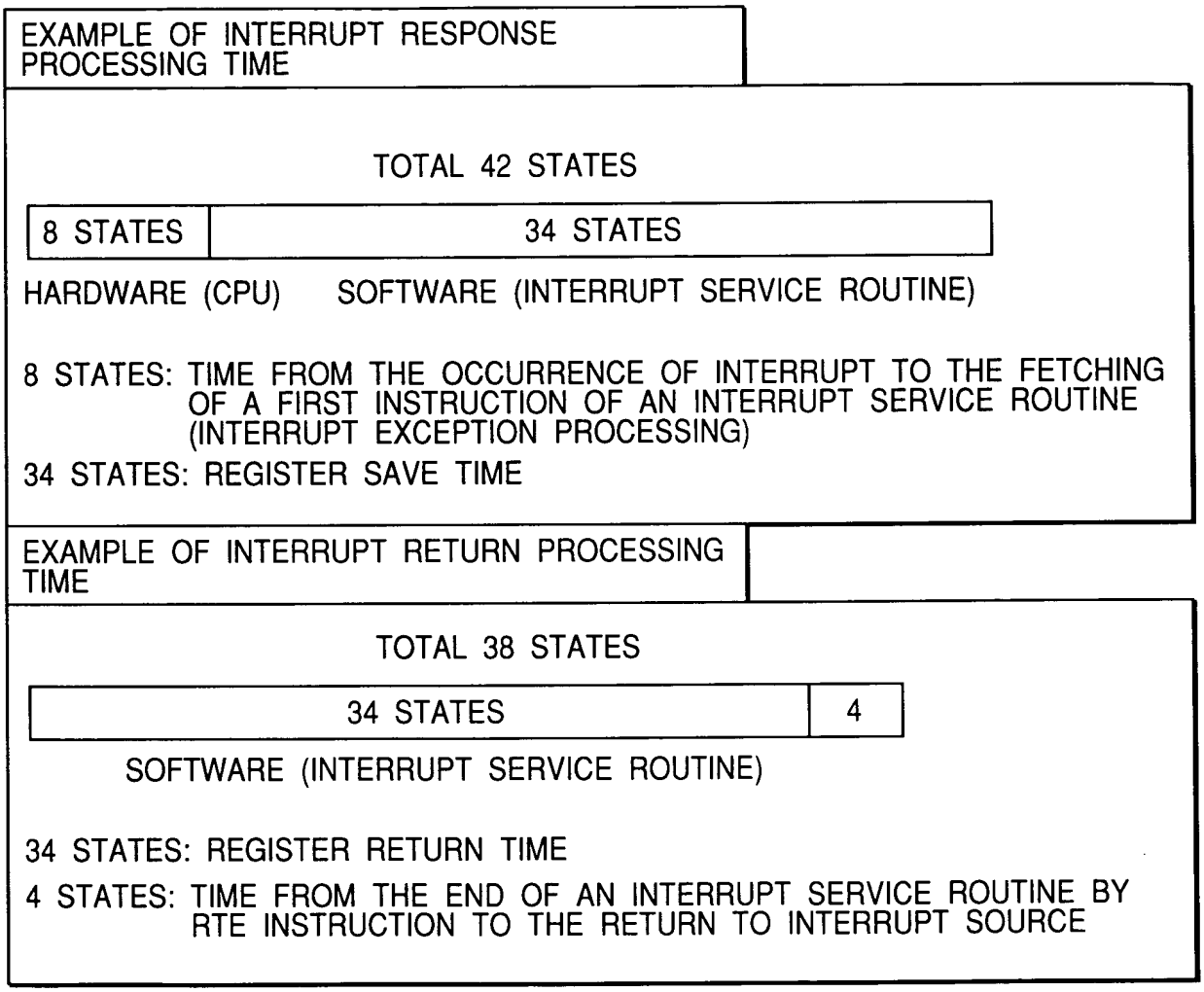
EXAMPLE OF INTERRUPT RESPONSE PROCESSING TIME
TOTAL 42 STATES
8 STATES
34 STATES
HARDWARE (CPU)
SOFTWARE (INTERRUPT SERVICE ROUTINE)
8 STATES: TIME FROM THE OCCURRENCE OF INTERRUPT TO THE FETCHING OF A FIRST INSTRUCTION OF AN INTERRUPT SERVICE ROUTINE (INTERRUPT EXCEPTION PROCESSING)
34 STATES: REGISTER SAVE TIME
EXAMPLE OF INTERRUPT RETURN PROCESSING TIME
TOTAL 38 STATES
34 STATES
4
SOFTWARE (INTERRUPT SERVICE ROUTINE)
34 STATES: REGISTER RETURN TIME
4 STATES: TIME FROM THE END OF AN INTERRUPT SERVICE ROUTINE BY RTE INSTRUCTION TO THE RETURN TO INTERRUPT SOURCE

FIG. 8

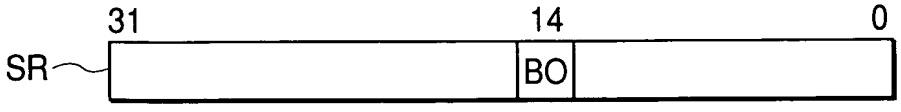
31
14
0
SR
BO

FIG. 9

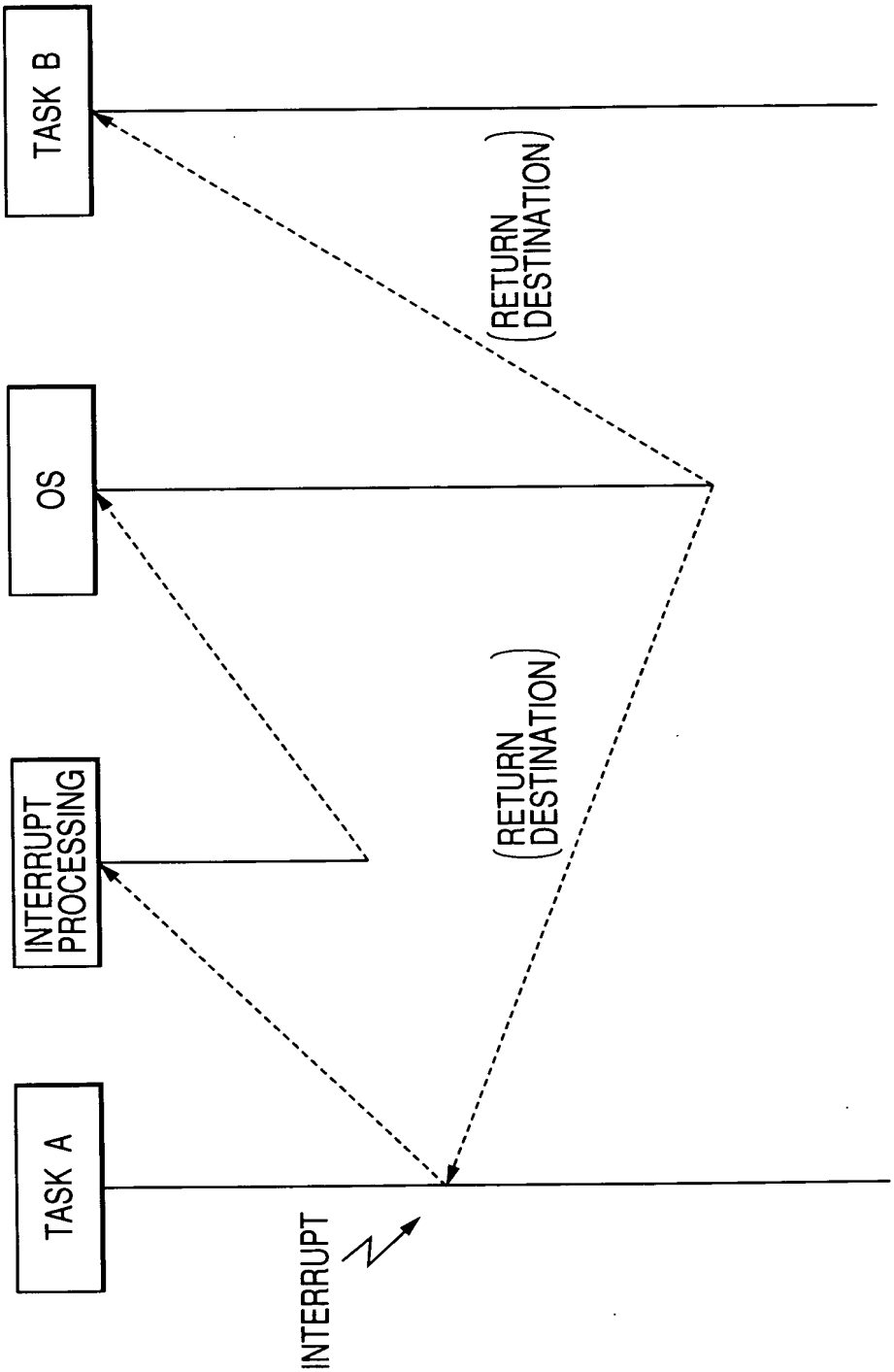
TASK B
OS
INTERRUPT PROCESSING
TASK A
INTERRUPT
(RETURN DESTINATION)
(RETURN DESTINATION)

FIG. 10

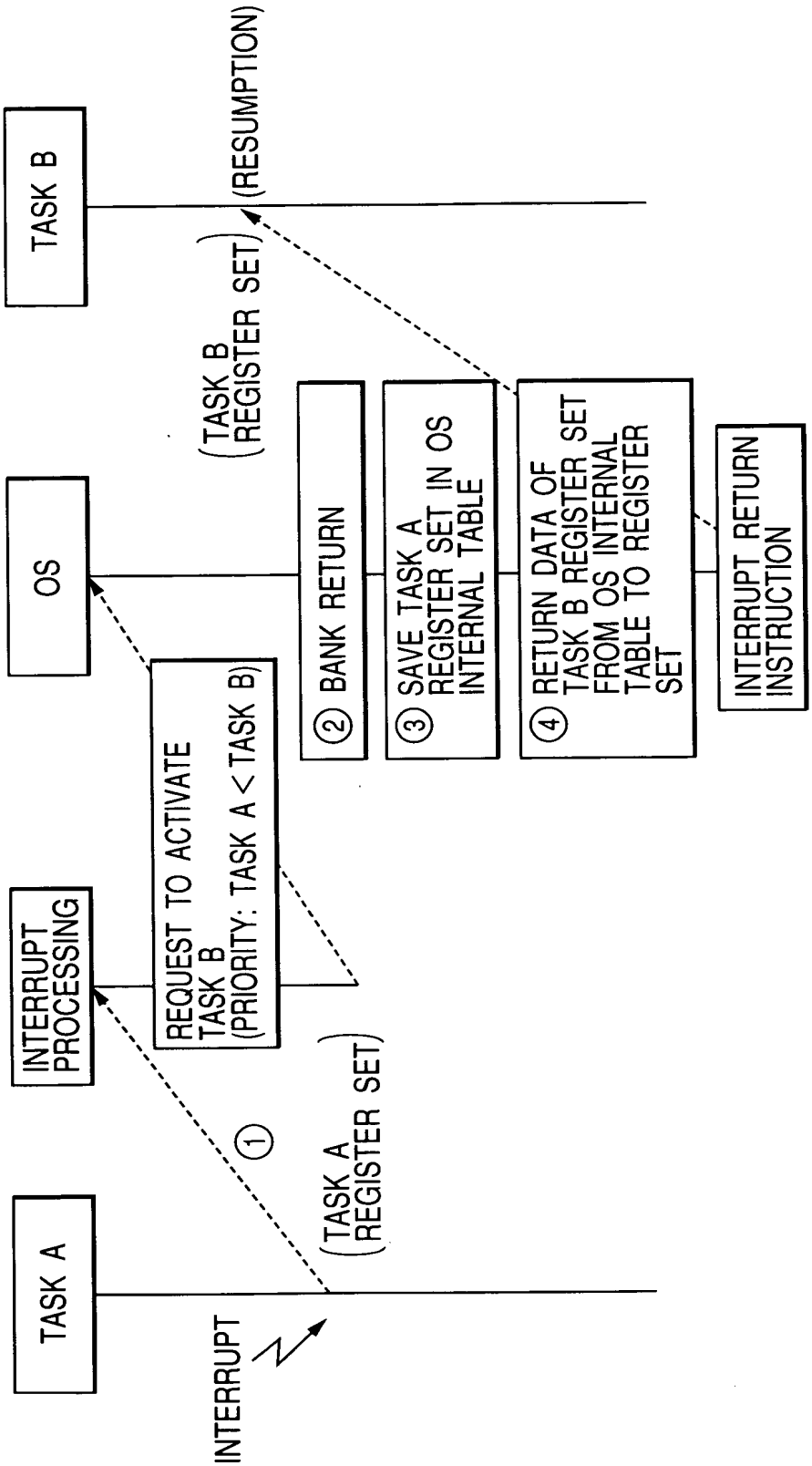
TASK A
TASK B
OS
INTERRUPT PROCESSING
INTERRUPT
(TASK A REGISTER SET)
①
REQUEST TO ACTIVATE TASK B (PRIORITY: TASK A < TASK B)
② BANK RETURN
(TASK B REGISTER SET)
③ SAVE TASK A REGISTER SET IN OS INTERNAL TABLE
④ RETURN DATA OF TASK B REGISTER SET FROM OS INTERNAL TABLE TO REGISTER SET
INTERRUPT RETURN INSTRUCTION
(RESUMPTION)

FIG. 11

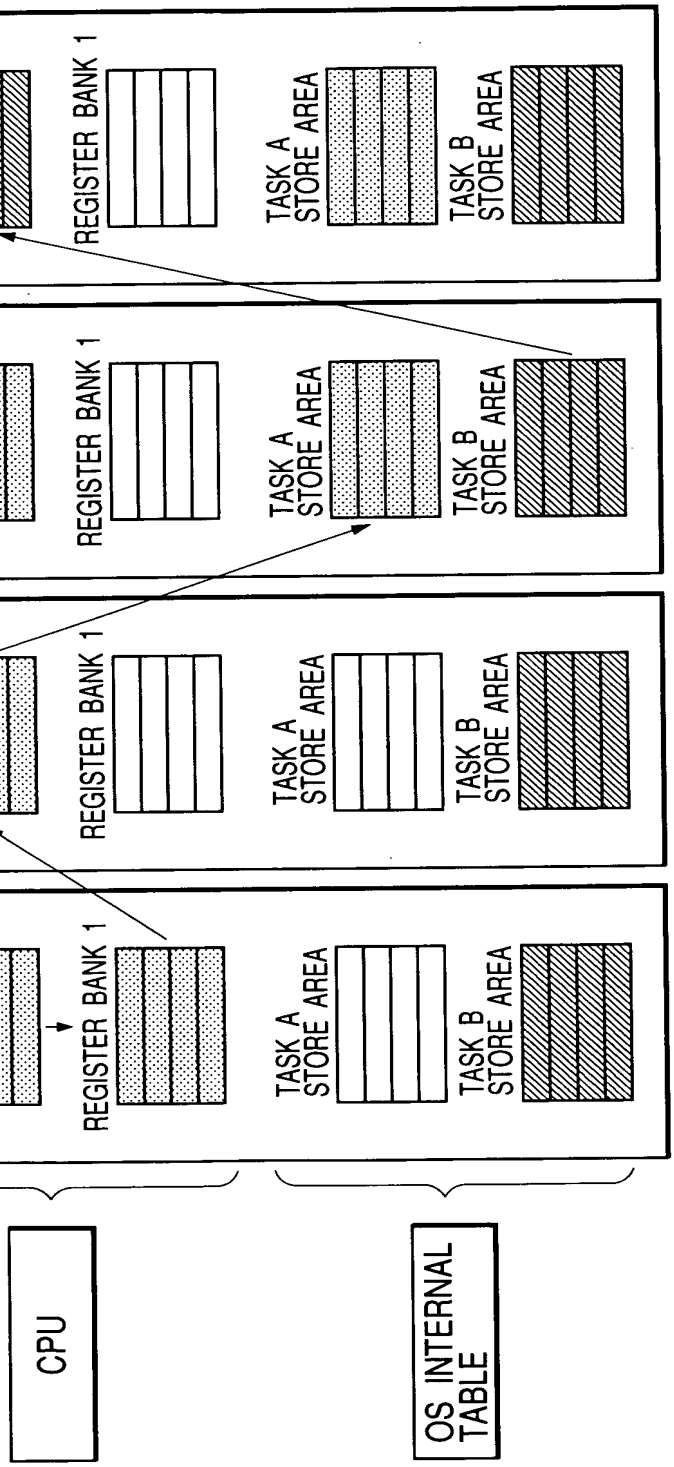
①
②
③
④
REGISTER SET
REGISTER BANK 1
TASK A STORE AREA
TASK B STORE AREA
CPU
OS INTERNAL TABLE

FIG. 12

MNEMONIC	OPERATION CONTENTS
LDBANK @Rm, R0	4-BYTE DATA FROM A REGISTER BANK ADDRESS INDICATED BY Rm IS TRANSFERRED TO R0
STBANK R0, @Rn	R0 IS TRANSFERRED TO A REGISTER BANK ADDRESS INDICATED BY Rn

FIG. 13